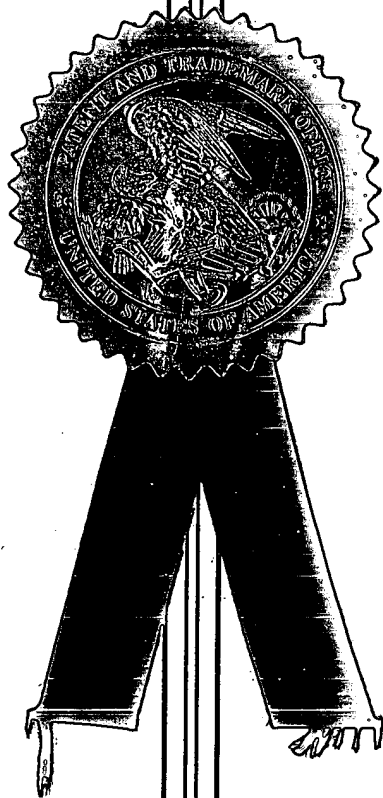


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Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.

If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the U.S. filing date, subject to any statutory extension. If the application contains a specific reference to an earlier filed application or applications under 35 U.S.C. 120, 121 or 365(c), the term of the patent is twenty years from the date on which the earliest application was filed, subject to any statutory extension.

J. Todd Pichini

Acting Commissioner of Patents and Trademarks

Allie M. Person
Attest

United States Patent [19]
Schaffer

[11] Patent Number: 5,870,296
[45] Date of Patent: Feb. 9, 1999

[54] DUAL INTERLEAVED DC TO DC SWITCHING CIRCUITS REALIZED IN AN INTEGRATED CIRCUIT

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[21] Appl. No.: 949,463

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[51] Int. Cl.⁶ H02M 7/00

[52] U.S. Cl. 363/65; 323/282

[58] Field of Search 323/282; 363/65, 363/26

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[57] ABSTRACT

Dual interleaved DC to DC switching circuits realizable in an integrated circuit form, capable of monitoring individual inductor current using only one current sense resistor and providing automatic duty cycle adjustment to keep the inductor currents in the interleaved DC to DC switching circuits balanced. The preferred embodiment includes a gain error amplifier, an integral error amplifier, and a differentiator error amplifier and circuits for controlling the nominal duty cycle, with the gain error amplifier, integral error amplifier and differentiator error amplifier being adjustable independently by external components. The circuit further includes a high speed load regulation circuit that momentarily overrides the control circuitry to take over control of the interleaved converters during sudden load changes, such control also being programmable. The circuit further includes a load variation circuit to target the output voltage of the circuit to an optimal value with load to better keep the output voltage within a targeted range in the event of major step changes in the load. The disclosed embodiment is for two interleaved buck converters, though the principles of the invention are applicable to interleaved step up converters and the interleaving of more than two converters.

21 Claims, 4 Drawing Sheets

2a	2b
2c	2d

